Paragraph 1 on page 1:

This application is a Divisional of U.S. Application No. 09/314,061, filed May 18, 1999, now U.S. Patent No. 6,226,295, which is a Divisional of U.S. Application No. 08/900,734, filed July 25, 1997, now U.S. Patent No. 5,907,591, which is a Continuation of U.S. Application No. 08/535,655, filed September 28, 1995, now U.S. Patent No. 5,666,390.

Paragraph 3 on page 1:

A United States Patent entitled "Self-Queing Serial Output Port" filed September 28, 1995, now issued as U.S. Patent No. 5,680,425, is assigned to the same assignee as the present application and is incorporated herein by reference.

Paragraph 1 on page 2:

A digital counter allows the provision of start and stop addresses in order to allow it to be configurable to any length, and to start and stop at desired positions in a cell of data. This provides a robust design that can easily be utilized in a larger circuit with little or no modification, minimizing design cost and complexity. In one embodiment, the counter rolls over to 0 after reaching a maximum value of 111 (112 cycles). The counter counts to 111 and then goes back to 0, continuing to count until it reaches an indicated stop count. At that point, it proceeds to the start count and continues counting. In this manner, the start count value may actually be higher than the stop count because the counter will just roll over and being counting at 0 until it reached the stop count.

Paragraph 1 on page 8:

Editing support for various cell lengths is accomplished by defining the ISAM start and stop positions within the ISAM's 56 byte space. The start and stop pointers are loaded by the command interface and command control 114, and are set such that the cell header appears in bytes 4-7 of the ISAM. The CRC byte, if present, is always in byte 8 of the ISAM. Figure 2 shows the ISAM space with the ATM cell header properly aligned. For the cases without any prepend/postpend data, Figure 3 show the ISAM start pointer set to 4 and the ISAM stop pointer set to 55 if no CRC is present (making a 52 byte cell). Similarly, Figure 4 shows the start pointer set to 4 if CRC is present (making a 53 byte cell).

The paragraph beginning on page 11, line 23:

The 7-bit count 526 of counter 510 is provided to a stop compare circuit indicated at 610 in Figure 6. Also provided as an input is a 7-bit stop signal on line 612. Each respective bit position of the count 526 and stop 612 signals is compared by Exclusive OR gates 614, 616, 618, 620, 622, 624, and 626, NOR gates 628 and 630, and NAND gate 632. The output of NAND gate 632 is inverted by an inverter 634 to provide a match signal on line 636 indicative of whether the stop signal 612 matches the count signal 616. The match signal 636 is utilized to trigger the load signal on line 536 in Figure 5, causing the value of the start signal on line 540 to be loaded into the latches. In operation, if any of the respective bits of the stop and count signals do not match, one of the Exclusive OR gates 614 through 626 provides a positive indication which is NORed by one of NOR gates 628 and 630, NANDed by NAND gate 632 and inverted to a non-positive indication of match by inverter 634. If all of the respective bits of the stop and count signals match, no positive indication is provided by the Exclusive OR gates, and a positive indication of match results on line 636. The end of each cell is identified by an input framing signal. If it is encountered prior to the stop signal, it is then known that there is an error in the cell. Parity data is also generated and stored in the DRAM to aid in checking cell integrity when the cell is transferred out of the DRAM.

The paragraph beginning on page 15, line 25:

In Figure 13, the control circuit 1220 is shown in more detail. Three latches, a STATUS latch 1310, a STOP latch 1312 and an OFRM latch or output frame signal generator 1314 operate to provide the signals associated with their names. A RESET signal provided on line 1316 is provided to each of the latches to reset them. A TRANSFER signal on line 1318 is provided to the STATUS latch 1310 to indicate to the control circuit that the output port has data to output to the channel. It causes a STATUS line 1320 to be raised.

The paragraph beginning on page 16, line 10 is amended as follows:

In operation, control circuit 1220 allows for a much simpler external controller. The controller only needs to check the STATUS signal of all of the ports on a bus or channel. If they are empty, meaning they do not contain a cell to be transferred to the bus, or one port is currently transferring data to the bus, as signified by STATUS=0, then it may transfer data into a port for later transfer onto the channel. If one port is full, STATUS=1, then that port is waiting to

transmit data. The control circuit is first reset by pulsing RESET on line 1316 hi, which sets it into input mode (OFRMDIR=0) and causes OFCLK 1328 to clock with the system clock SCLK on line 1340. If no chip has yet had a transfer, all the ports coupled to the channel will have OFRMDIR=0, and the OFCLK signal enabled to clock with SCLK. A transfer command from the switch is signified by TRANSFER 1318 pulsing high, which sets the STATUS latch 1310, then OFCLK clocks STATUS into the flip flop 1330 setting OFRMDIR 1332 high, which feeds back to reset the STATUS latch. OFRMDIR* feeds into a NOR gate 1342, which sets the OFRM latch 1314 high. OFRM is then set low on the next SCLK due to feedback through a NAND gate 1344, and then sets the OFCLK latch so that OFCLK will not fire. A new TRANSFER initiated by the external controller stays in the STATUS latch until OFCLK is re-enabled. The OFRM hi will start the counter going in all of the ports, but only the port with OFRMDIR hi will have it's data and OFRM outputs enabled to allow cell data to be clocked out to the channel. When the control circuit then outputs OFRM hi for one cycle, it disables the OFCLK on the other ports (OFRMIN pulses hi), and starts their counters. When all of the ports reach the last bit of data (STOP pulses hi), then the OFCLK is enabled again, so the port that was in output mode will clock in a 0, setting OFRMDIR=0, while the port with STATUS set by the external controller clocks that in, setting it's OFRMDIR hi and allowing it to transfer data starting on the next available cycle.